PATENT
Atty Docket No.: 10004808-1

In The U.S. Patent and Trademark Office

In Re the Application of:

Inventor(s):	Osamu S. Nakagawa	**Confirmation No.:**	3635
Serial No.:	09/891,324	**Examiner:**	Schillinger, Laura M.
Filed:	June 27, 2001	**Group Art Unit:**	2813

Title: PROCESS FOR HIGH-DIELECTRIC CONSTANT METAL-INSULATOR METAL CAPACITOR IN VLSI MULTI-LEVEL METALLIZATION SYSTEMS

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1 sheet of Transmittal Letter for Appeal Brief (2 copies).

18 sheets of Appeal Brief including Appendices.

Respectfully submitted,

MANNAVA & KANG, P.C.

November 14, 2005

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PATENT APPLICATION

ATTORNEY DOCKET NO. 10004808-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

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TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on August 19, 2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Number of pages: 21

Respectfully submitted,

Osamu S. Nakagawa

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Number of pages: 21

Typed Name: Judy H. Chung

Respectfully submitted,

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APPEAL BRIEF

Appellants respectfully submit this Appeal Brief in response to the final Official Action mailed on March 8, 2005, the Advisory Action mailed on June 21, 2005, and the Notice of Panel Decision from Pre-Appeal Brief Review mailed on October 14, 2005.

The present Appeal Brief is being filed within one month of the Notice of Panel Decision from Pre-Appeal Brief Review.

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Art Unit: 2813

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I. INTRODUCTION

A. Real Party in Interest

The real party in interest with respect to this appeal is the Hewlett-Packard Company, the named assignee in this application.

B. Related Appeals and Interferences

None.

C. Status of Claims

Claims 1-13 stand rejected, and Claims 1-13 are at issue on this appeal.

Pursuant to 37 C.F.R. § 41.37, Appellant hereby appeals the Examiner's decision finally rejecting Claims 1-13 to the Board of Patent Appeals and Interferences. Therefore, all claims pending in this application are at issue on this appeal.

D. Status of Amendments

A Request for Reconsideration was filed subsequent to the issuance of the final Office Action. That Request for Reconsideration did not include any amendments to the claims.

A copy of the claims at issue on appeal is attached as the Claims Appendix.

II. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 of the present invention is the only independent claim and pertains to a method of forming a by-pass capacitor on a multi-level metallization device (100), as shown in the flow diagram (200) depicted in Figure 2. The steps outlined in the flow diagram (200)

are further illustrated with respect to Figures 3A-3E, which depict side views during various stages of the claimed multi-level metallization device (100) formation process.

In the method of Claim 1, a first electrode (320-324) is formed in a first dielectric layer (305) of the multi-level metallization device (100). This element of Claim 1 is depicted at step 210 of Figure 2, in Figure 3A, and a description of this element is set forth in line 14 of page 7 to line 2 of page 8 in the *Specification*.

In addition, Claim 1 includes that a substantially thin insulator layer (330) is deposited over the first dielectric layer (305) of the multi-level metallization device (100). This feature of Claim 1 is depicted at step 215 of Figure 2, in Figure 3B, and a description of this element is set forth in lines 3-12 of page 8 of the *Specification*.

Claim 1 further includes that a second electrode (360) is formed in a second dielectric layer (335), wherein the second dielectric layer (335) is formed over the substantially thin insulator layer (330). This feature of Claim 1 is depicted at step 235 of Figure 2, in Figure 3E, and a description of this element is set forth in the paragraph starting on line 21 of page 8 and ending on line 2 of page 9 of the *Specification*.

III. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4 and 7-13 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by the disclosure contained in U.S. Patent No. 6,051,858 to Uchida et al.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,051,858 to Uchida et al.

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IV. ARGUMENT

A. Rejection of Claims 1-4 and 7-13 Under 35 U.S.C. §102 Over U.S. Patent No. 6,051,858 to Uchida et al.

1. The Examiner's Position

The Examiner is of the opinion that U.S. Patent No. 6,051,858 to Uchida et al. (herein after "Uchida et al.") discloses all of the features claimed in Claims 1-4 and 7-13 of the present invention and that Claims 1-4 and 7-13 are therefore anticipated by the disclosure contained in Uchida et al. In setting forth this rejection, the Examiner alleges that Figure 5 of Uchida et al. discloses all of the features claimed in Claims 1-4 and 7-13 of the present invention. A copy of Figure 5 is reproduced below.

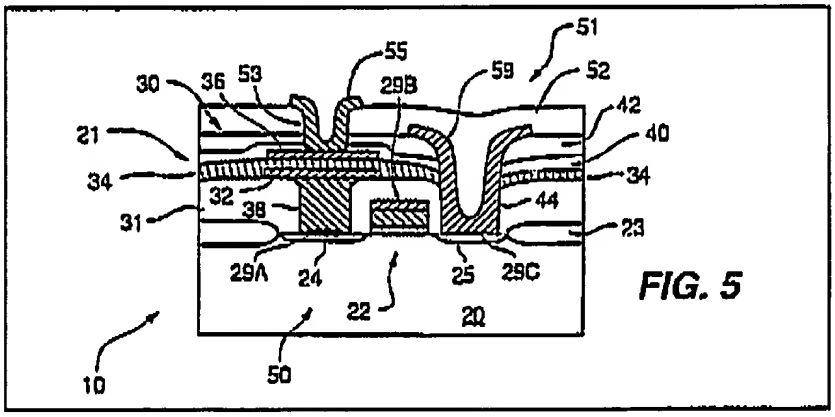

FIG. 5

The Examiner alleges that the bottom electrode (32) and the ferroelectric/dielectric layer (34) of Uchida et al. respectively read on the claimed first electrode (320-324) and the claimed first dielectric layer (305). The Examiner also alleges that Uchida et al. discloses a step of forming the bottom electrode (32) in the ferroelectric/dielectric layer (34).

In addition, the Examiner alleges that the ferroelectric/dielectric layer (34) of Uchida et al. reads on the claimed substantially thin dielectric material layer (330). In this regard, the

Examiner also alleges that Uchida et al. discloses depositing the ferroelectric/dielectric layer (34) over the ferroelectric/dielectric layer (34). In other words, the Examiner has alleged that Figure 5 of Uchida et al. somehow discloses that the ferroelectric/dielectric layer (34) is deposited on itself. In making this allegation, the Examiner has also asserted that Uchida et al. somehow discloses that the bottom electrode (32) is formed in the ferroelectric/dielectric layer (34) and that the ferroelectric/dielectric layer (34) is deposited on the ferroelectric/dielectric layer (34).

The Examiner has apparently recognized this deficiency in Uchida et al., but has argued on pages 5 and 6 of the Official Action mailed on March 8, 2005, that "element 34 ***could be*** divided into two layers the lower layer has a dielectric layer formed in it. The upper portion of element 34 meets the requirements of Applicant's claim language in that it lies over the lower portion of 34. Therefore Uchida anticipates Applicant's claim language." *Emphasis added.* The Examiner is thus of the opinion that the ferroelectric/dielectric layer 34 of Uchida et al. ***could be modified to anticipate*** the claimed invention.

Furthermore, the Examiner asserts that a wiring layer (55) and protective layer (40) of Uchida et al. respectively read on the claimed second electrode (360) and the claimed second dielectric layer (335). The Examiner also asserts that the wiring layer (55) is formed substantially over the protective layer (40).

2. Discussion of the Law

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way

to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

> Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

3. The Appellant's Position

The rejection of Claims 1-4 and 7-13 based upon the disclosure contained in Uchida et al. is improper and should be withdrawn for at least the following reasons.

a. *Interpretation of Uchida et al. is Clearly Incorrect*

Initially, the assertion that the protective layer 40 of Uchida et al. reads on the second dielectric layer 335 of Claim 1 is incorrect because the protective layer 40 is not a dielectric layer. Instead, the protective layer 40 "comprises one or more metals with oxygen and/or nitrogen." Column 9, lines 28-30 of Uchida et al. As such, the protective layer 40 appears to be a conductor of electricity and not an insulator of electricity. As such, the Examiner's allegation that the protective layer 40 is a dielectric layer is incorrect.

In addition, the assertion that the ferroelectric/dielectric layer 34 is deposited over the ferroelectric/dielectric layer 34 to read on "depositing a substantially thin insulator layer over

said first dielectric layer" is improper because a single layer 34 cannot reasonably be construed as being deposited over itself. As shown very clearly in Figure 5 of Uchida et al., the ferroelectric/dielectric layer 34 comprises a **single layer** that is most likely deposited during a single deposition operation and not formed as separate layers. Therefore, there appears to be absolutely no disclosure in Uchida et al. to lead one to conclude that the ferroelectric/dielectric layer 34 is deposited over itself as separate layers.

Moreover, Uchida et al. fails to disclose that a first electrode is formed in a first dielectric layer. Instead, Figures 3 and 4 of Uchida et al. appear to show that the bottom electrode 32 is formed or placed over a plug 38 and then the ferroelectric/dielectric layer 34 is formed over the bottom electrode 32. As such, Uchida et al. fails to disclose the step of forming the bottom electrode 32 in the ferroelectric/dielectric layer 34.

For at least these reasons, the allegation that Uchida et al. anticipates Claim 1 is improper and should be withdrawn.

b. *Anticipation Rejection is Clearly Improper*

Even assuming for the sake of argument that the above-described interpretation of Uchida et al. is proper, the proposed interpretation would still fail to disclose each and every element claimed in Claim 1. For instance, Uchida et al. fails to disclose forming a first electrode in a first dielectric layer and depositing a substantially thin insulator layer over the first dielectric layer, as recited in Claim 1. Instead, Uchida et al. shows in Figures 3-5, that the bottom electrode 32 is formed or deposited over a plug 38 and that the ferroelectric/dielectric layer 34 is, in most likelihood, deposited on top of the bottom electrode 32.

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The Official Action acknowledges that Uchida et al. does not disclose depositing a substantially thin insulator layer over the first dielectric layer in the "Response to Arguments" section on pages 5 and 6 of the Official Action mailed on March 8, 2005. More particularly, the Official Action asserts that the ferroelectric/dielectric layer 34 "could be divided into two layers has[*sic*] a dielectric layer formed on it. The upper portion of element 34 meets the requirements of Applicant's claim language in that it lies over the lower portion of 34." Basically, therefore, the Official Action has asserted that the ferroelectric/dielectric layer 34 of Uchida et al. **could be** divided into two layers. There are, however, a number of errors and improprieties associated with this assertion.

Firstly, the assertion that Uchida et al. could be modified to divide the ferroelectric/dielectric layer 34 into two layers is an improper basis for setting forth a rejection based upon anticipation. Anticipation cannot be based on what "could be" taught by the reference or what might be taught through modification of a reference. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

> Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Here, by the Examiner's own admission, Uchida et al. fails to disclose each and every element claimed in Claim 1. As such, Uchida et al. fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over Uchida et al.

Secondly, even assuming for the sake of argument the Official Action intended to reject Claim 1 as being obvious, the Official Action has not provided any reason or

motivation to lead one of ordinary skill in the art to divide the ferroelectric/dielectric layer 34 of Uchida et al. into two layers. In addition, there appears to be no disclosure in Uchida et al. to lead one of ordinary skill in the art to modify Uchida et al. as proposed in the Official Action. More particularly, there appears to be no disclosure in Uchida et al. to apply the single ferroelectric/dielectric layer 34 of Uchida et al. as two separate layers in two separate steps. Therefore, the present invention as claimed in Claim 1 would be unobvious over the disclosure contained in Uchida et al.

It is thus respectfully submitted that Uchida et al. fails to anticipate the claimed invention as set forth in Claim 1 and that the Examiner has improperly rejected Claim 1.

For at least the foregoing reasons, the rejection of Claim 1 is clearly improper and should be withdrawn.

B. Rejection of Claims 5 and 6 Under 35 U.S.C. §103 Over U.S. Patent No. 6,051,858 to Uchida et al.

1. The Examiner's Position

The Examiner has rejected Claims 5 and 6 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the disclosure contained in Uchida et al.

More particularly, the Examiner has rejected Claims 5 and 6 as being *prima facie* obvious in view of the disclosure contained in Uchida et al. because the ranges claimed in Claims 5 and 6 have allegedly not been shown to achieve unexpected results.

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2. Discussion of the Law

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

3. The Appellant's Position

The rejection of Claims 5 and 6 based upon the disclosure contained in Uchida et al. is improper and should be withdrawn for at least the following reasons.

The Official Action correctly notes that Uchida et al. fails to explicitly teach the thickness of the thin insulator layer as claimed in Claim 5 of the present invention. However, the Official Action incorrectly concludes that the passage recited in lines 45-50 of column 14 discloses that the ferroelectric/dielectric layer 34 is thin. Instead, this cited passage discusses that an active layer 106 is a thin film and therefore does not appear to pertain to the ferroelectric/dielectric layer 34 cited above. Thus, the reliance on this cited passage to somehow conclude that a *prima facie* case of obviousness has been achieved is improper.

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The Official Action also correctly notes that Uchida et al. fails to disclose that the dielectric constant of the substantially thin insulator layer is between 4 and 100. However, the Official Action incorrectly concludes that Claim 6 is *prima facie* obvious because there does not appear to be any indication in Uchida et al. that suggests that the dielectric constant of the substantially thin insulator layer is between 4 and 100.

Even assuming for the sake of argument, however, that the bases for concluding that Claims 5 and 6 are somehow rendered obvious by the disclosure contained in Uchida et al. is proper, the proposed justifications do not purport to render independent Claim 1 unpatentable over Uchida et al. In fact, Uchida et al. still fails to disclose all of the features of allowable Claim 1 upon which Claims 5 and 6 depend. Accordingly, Claims 5 and 6 are allowable over Uchida et al. at least by virtue of their dependencies upon allowable Claim 1.

For at least the foregoing reasons, the proposed modification to Uchida et al. fails to render Claims 5 and 6 obvious.

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V. CONCLUSION

For at least the reasons set forth above, it is respectfully submitted that the rejection of Claims 1-13 is improper. The Appellant therefore respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting Claims 1-13 and to direct the Examiner to pass the case to issue.

Respectfully submitted,

Guillermo A. Alvarez et al.

Dated: November 14, 2005 By

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CLAIMS APPENDIX

The Appealed Claims:

1. A method of forming a by-pass capacitor on a multi-level metallization device, said method comprising:

forming a first electrode in a first dielectric layer of said multi-level metallization device;

depositing a substantially thin insulator layer over said first dielectric layer of said multi-level metallization device; and

forming a second electrode in a second dielectric layer, wherein said second dielectric layer is formed over said substantially thin insulator layer.

2. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, said method further comprising:

patterning said substantially thin insulator layer to substantially cover said first electrode; and

adjusting a thickness of said substantially thin insulator layer.

3. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 2, wherein a dielectric constant of said substantially thin insulator layer is substantially high.

4. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said substantially thin insulator layer includes silicon nitride.

5. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said thickness of said substantially thin insulator layer is between 50 and 100 angstroms.

6. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 3, wherein said dielectric constant of said substantially thin insulator layer is between 4 and 100.

7. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, said method further comprising:

depositing the second dielectric layer over said substantially thin insulator layer; and

etching at least one via, said at least one via adapted to receive said second electrode.

8. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 7, said method further comprising:

polishing said second electrode.

9. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, wherein said forming said first electrode comprises:

etching said first electrode in the first dielectric layer of said multi-level metallization device.

10. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, further comprising:

forming the first electrode in a parallel line configuration.

11. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, further comprising:

forming the second electrode in a parallel line configuration.

12. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 1, wherein said substantially thin insulator layer comprises a composite of materials.

13. The method of forming a by-pass capacitor on a multi-level metallization device according to claim 12, wherein said composite of materials includes PZT and platinum.

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EVIDENCE APPENDIX

No evidence is submitted herewith.

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RELATED PROCEEDINGS APPENDIX

No copies of decisions rendered by a court of the Board are submitted herewith.